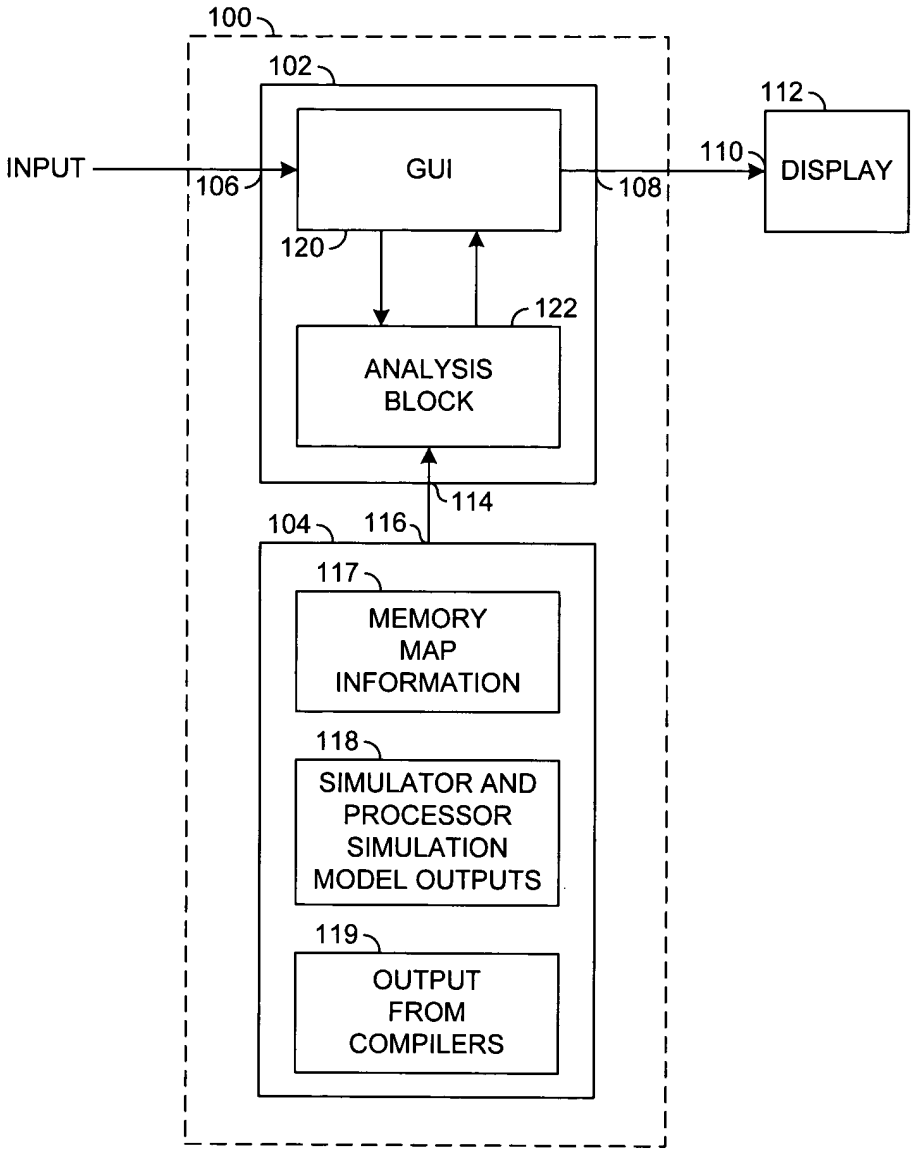
100
102
112
INPUT
GUI
110
DISPLAY
106
108
120
122
ANALYSIS BLOCK
114
104
116
117
MEMORY MAP INFORMATION
118
SIMULATOR AND PROCESSOR SIMULATION MODEL OUTPUTS
119
OUTPUT FROM COMPILERS

FIG. 1

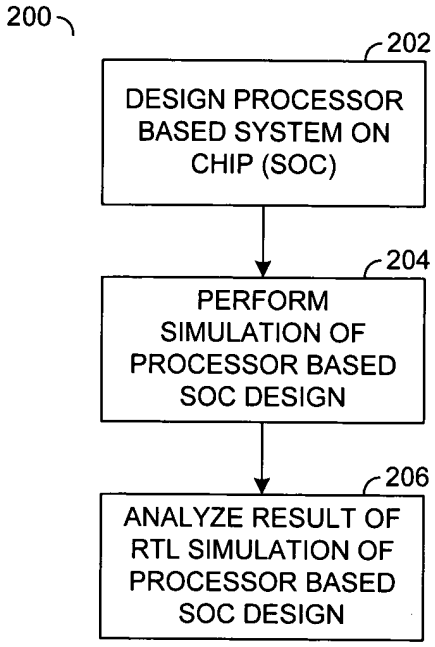
200
202
DESIGN PROCESSOR BASED SYSTEM ON CHIP (SOC)
204
PERFORM SIMULATION OF PROCESSOR BASED SOC DESIGN
206
ANALYZE RESULT OF RTL SIMULATION OF PROCESSOR BASED SOC DESIGN

FIG. 2

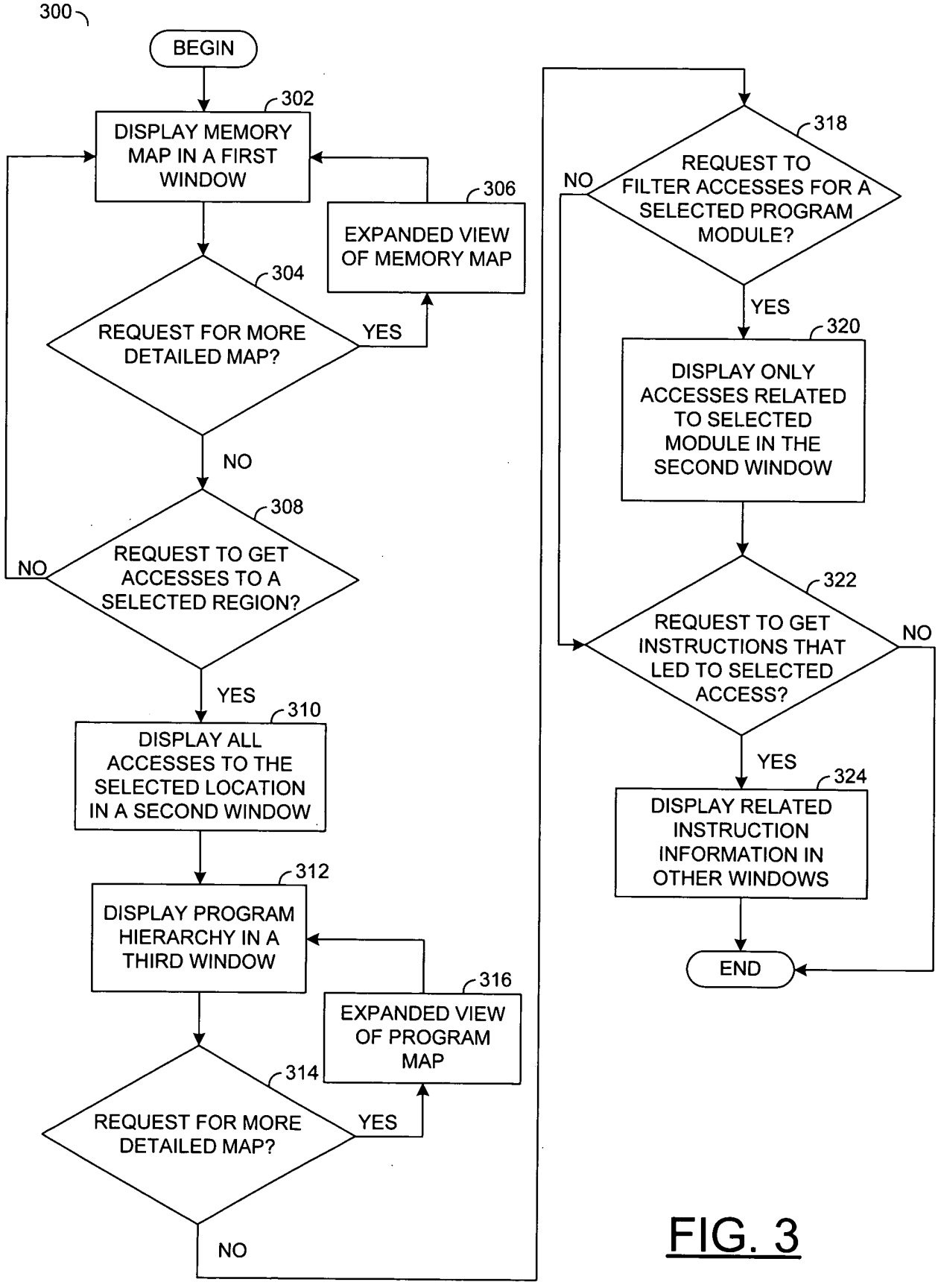
300
BEGIN
302
DISPLAY MEMORY MAP IN A FIRST WINDOW
306
EXPANDED VIEW OF MEMORY MAP
304
REQUEST FOR MORE DETAILED MAP?
YES
NO
308
REQUEST TO GET ACCESSES TO A SELECTED REGION?
NO
YES
310
DISPLAY ALL ACCESSES TO THE SELECTED LOCATION IN A SECOND WINDOW
312
DISPLAY PROGRAM HIERARCHY IN A THIRD WINDOW
316
EXPANDED VIEW OF PROGRAM MAP
314
REQUEST FOR MORE DETAILED MAP?
YES
NO
318
REQUEST TO FILTER ACCESSES FOR A SELECTED PROGRAM MODULE?
NO
YES
320
DISPLAY ONLY ACCESSES RELATED TO SELECTED MODULE IN THE SECOND WINDOW
322
REQUEST TO GET INSTRUCTIONS THAT LED TO SELECTED ACCESS?
NO
YES
324
DISPLAY RELATED INSTRUCTION INFORMATION IN OTHER WINDOWS
END

FIG. 3

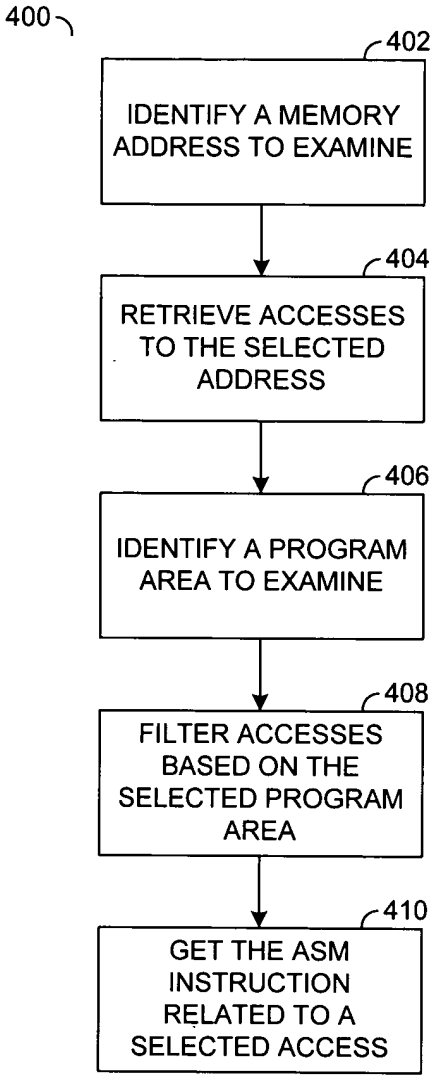
400
402
IDENTIFY A MEMORY ADDRESS TO EXAMINE
404
RETRIEVE ACCESSES TO THE SELECTED ADDRESS
406
IDENTIFY A PROGRAM AREA TO EXAMINE
408
FILTER ACCESSES BASED ON THE SELECTED PROGRAM AREA
410
GET THE ASM INSTRUCTION RELATED TO A SELECTED ACCESS

FIG. 4

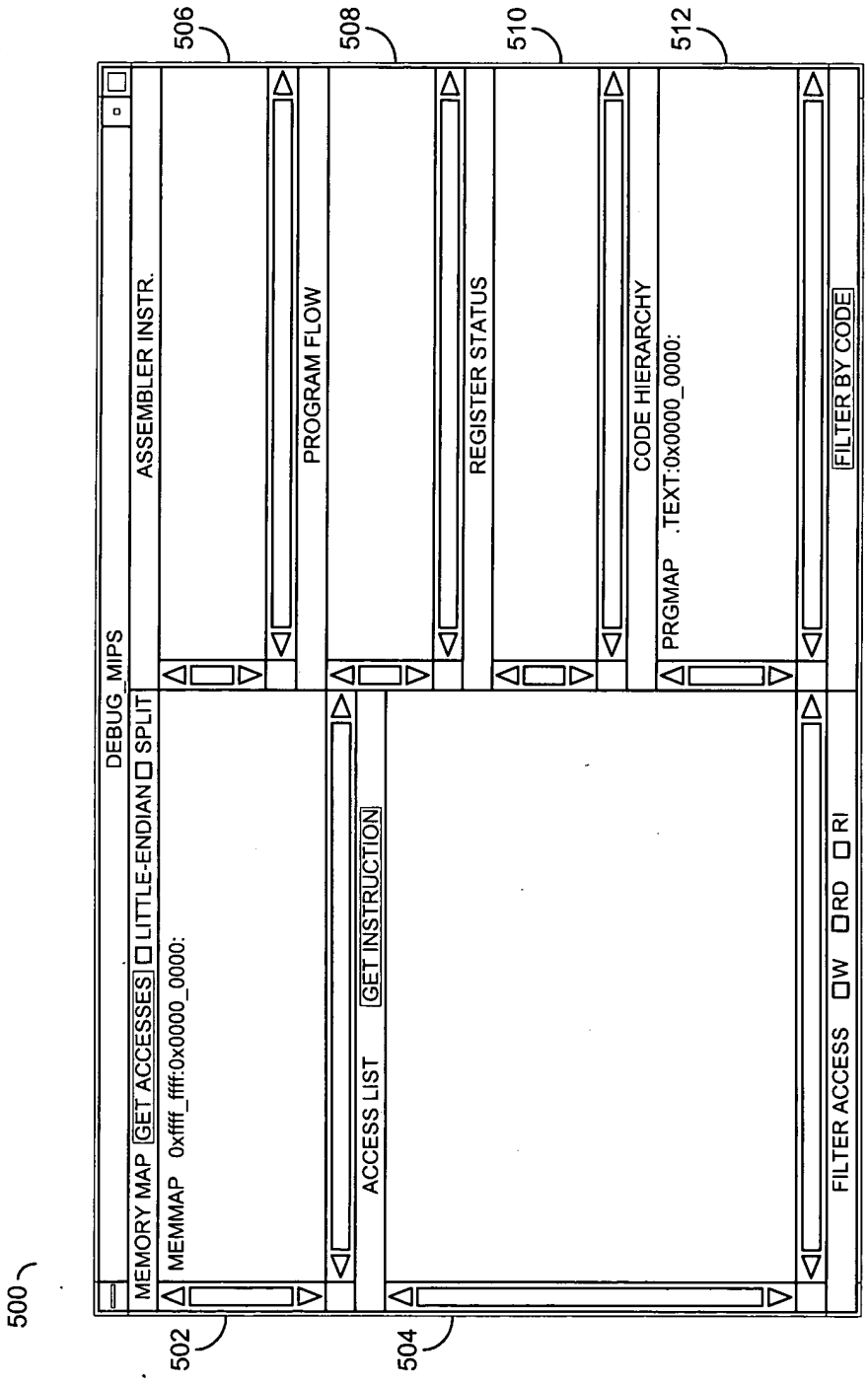
500
DEBUG_MIPS
MEMORY MAP
GET ACCESSES
LITTLE-ENDIAN
SPLIT
MEMMAP 0xffff_ffff:0x0000_0000:
ASSEMBLER INSTR.
PROGRAM FLOW
REGISTER STATUS
CODE HIERARCHY
PRGMAP .TEXT:0x0000_0000:
ACCESS LIST
GET INSTRUCTION
FILTER ACCESS
W
RD
RI
FILTER BY CODE
502
504
506
508
510
512

FIG. 5

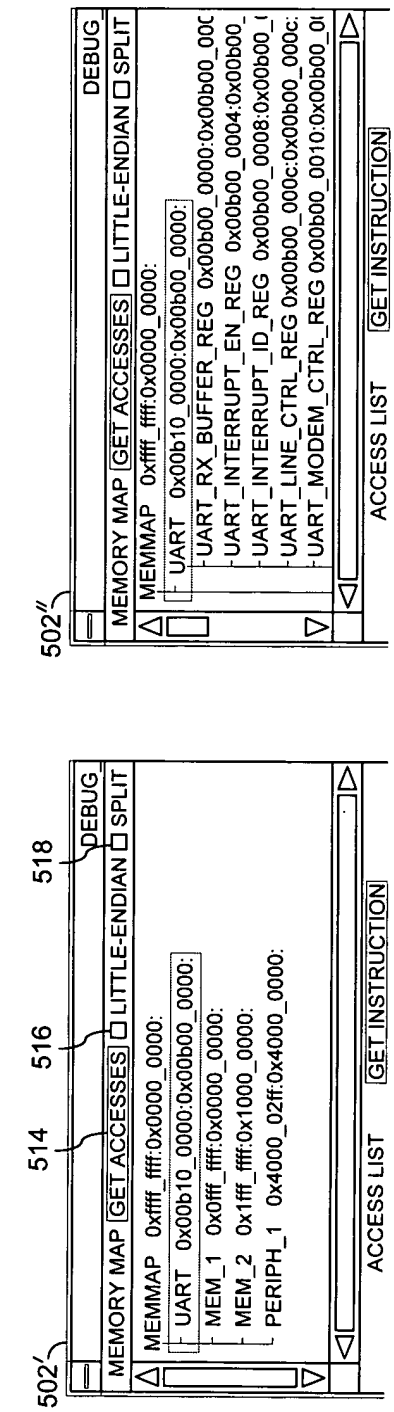
502'
514
516
518
DEBUG
MEMORY MAP
GET ACCESSES
LITTLE-ENDIAN
SPLIT
MEMMAP 0xffff_ffff:0x0000_0000:
UART 0x00b10_0000:0x00b00_0000:
MEM_1 0x0fff_ffff:0x0000_0000:
MEM_2 0x1fff_ffff:0x1000_0000:
PERIPH_1 0x4000_02ff:0x4000_0000:
ACCESS LIST
GET INSTRUCTION
502''
DEBUG
MEMORY MAP
GET ACCESSES
LITTLE-ENDIAN
SPLIT
MEMMAP 0xffff_ffff:0x0000_0000:
UART 0x00b10_0000:0x00b00_0000:
UART_RX_BUFFER_REG 0x00b00_0000:0x00b00_00C
UART_INTERRUPT_EN_REG 0x00b00_0004:0x00b00_
UART_INTERRUPT_ID_REG 0x00b00_0008:0x00b00_1
UART_LINE_CTRL_REG 0x00b00_000c:0x00b00_000c:
UART_MODEM_CTRL_REG 0x00b00_0010:0x00b00_0I
ACCESS LIST
GET INSTRUCTION

FIG. 6

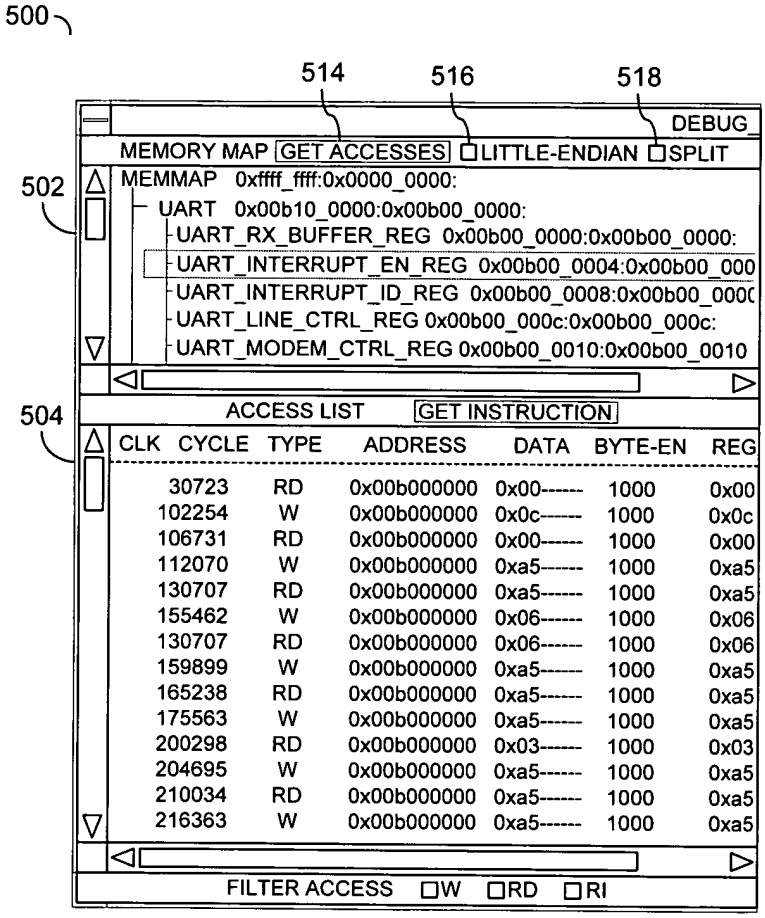
500
514
516
518
DEBUG
MEMORY MAP GET ACCESSES LITTLE-ENDIAN SPLIT
502
MEMMAP 0xffff_ffff:0x0000_0000:
UART 0x00b10_0000:0x00b00_0000:
UART_RX_BUFFER_REG 0x00b00_0000:0x00b00_0000:
UART_INTERRUPT_EN_REG 0x00b00_0004:0x00b00_000
UART_INTERRUPT_ID_REG 0x00b00_0008:0x00b00_000(
UART_LINE_CTRL_REG 0x00b00_000c:0x00b00_000c:
UART_MODEM_CTRL_REG 0x00b00_0010:0x00b00_0010
504
ACCESS LIST GET INSTRUCTION
CLK CYCLE TYPE ADDRESS DATA BYTE-EN REG
30723 RD 0x00b000000 0x00------ 1000 0x00
102254 W 0x00b000000 0x0c------ 1000 0x0c
106731 RD 0x00b000000 0x00------ 1000 0x00
112070 W 0x00b000000 0xa5------ 1000 0xa5
130707 RD 0x00b000000 0xa5------ 1000 0xa5
155462 W 0x00b000000 0x06------ 1000 0x06
130707 RD 0x00b000000 0x06------ 1000 0x06
159899 W 0x00b000000 0xa5------ 1000 0xa5
165238 RD 0x00b000000 0xa5------ 1000 0xa5
175563 W 0x00b000000 0xa5------ 1000 0xa5
200298 RD 0x00b000000 0x03------ 1000 0x03
204695 W 0x00b000000 0xa5------ 1000 0xa5
210034 RD 0x00b000000 0xa5------ 1000 0xa5
216363 W 0x00b000000 0xa5------ 1000 0xa5
FILTER ACCESS W RD RI

FIG. 7

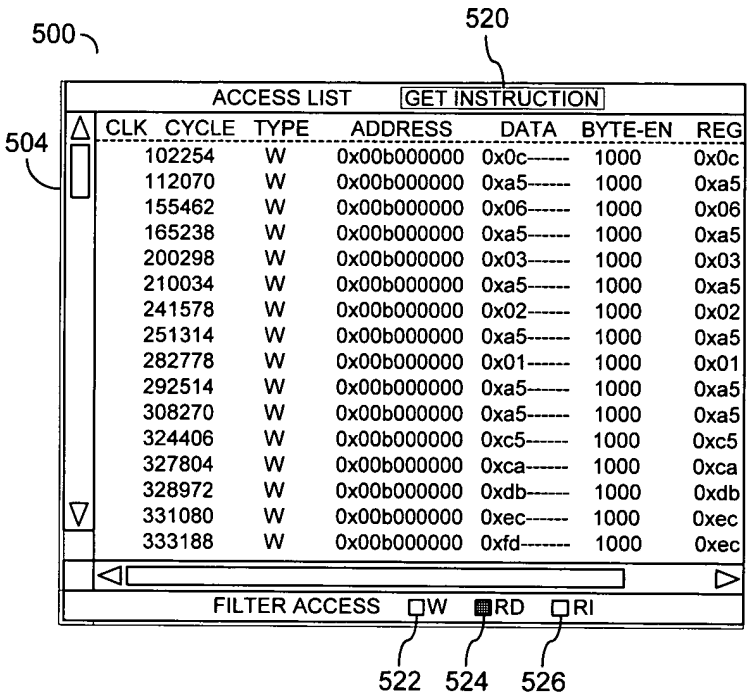
500
520
504
ACCESS LIST
GET INSTRUCTION
CLK CYCLE TYPE ADDRESS DATA BYTE-EN REG
102254 W 0x00b000000 0x0c------ 1000 0x0c
112070 W 0x00b000000 0xa5------ 1000 0xa5
155462 W 0x00b000000 0x06------ 1000 0x06
165238 W 0x00b000000 0xa5------ 1000 0xa5
200298 W 0x00b000000 0x03------ 1000 0x03
210034 W 0x00b000000 0xa5------ 1000 0xa5
241578 W 0x00b000000 0x02------ 1000 0x02
251314 W 0x00b000000 0xa5------ 1000 0xa5
282778 W 0x00b000000 0x01------ 1000 0x01
292514 W 0x00b000000 0xa5------ 1000 0xa5
308270 W 0x00b000000 0xa5------ 1000 0xa5
324406 W 0x00b000000 0xc5------ 1000 0xc5
327804 W 0x00b000000 0xca------ 1000 0xca
328972 W 0x00b000000 0xdb------ 1000 0xdb
331080 W 0x00b000000 0xec------ 1000 0xec
333188 W 0x00b000000 0xfd------- 1000 0xec
FILTER ACCESS W RD RI
522 524 526

FIG. 8

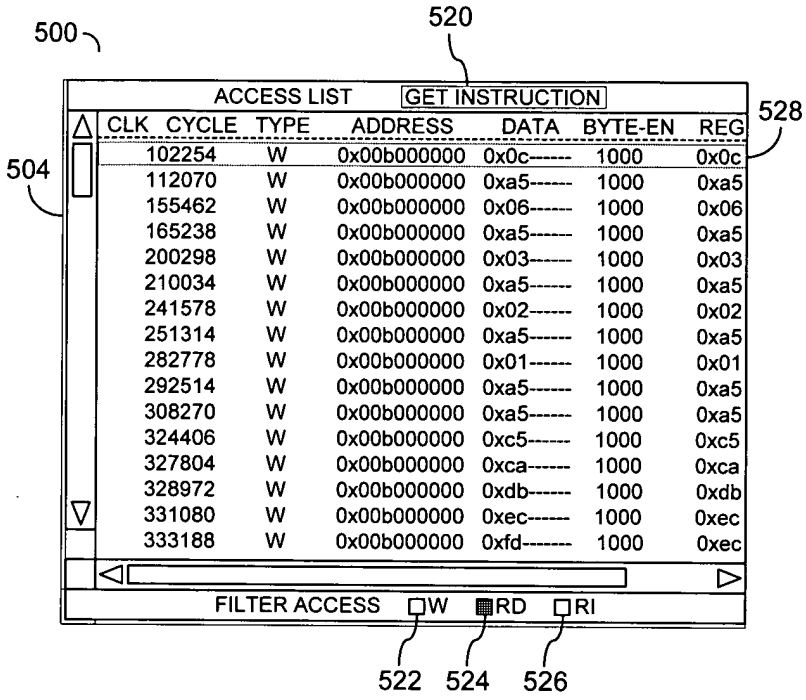
500
520
ACCESS LIST
GET INSTRUCTION
528
504
CLK CYCLE TYPE ADDRESS DATA BYTE-EN REG
102254 W 0x00b000000 0x0c------ 1000 0x0c
112070 W 0x00b000000 0xa5------ 1000 0xa5
155462 W 0x00b000000 0x06------ 1000 0x06
165238 W 0x00b000000 0xa5------ 1000 0xa5
200298 W 0x00b000000 0x03------ 1000 0x03
210034 W 0x00b000000 0xa5------ 1000 0xa5
241578 W 0x00b000000 0x02------ 1000 0x02
251314 W 0x00b000000 0xa5------ 1000 0xa5
282778 W 0x00b000000 0x01------ 1000 0x01
292514 W 0x00b000000 0xa5------ 1000 0xa5
308270 W 0x00b000000 0xa5------ 1000 0xa5
324406 W 0x00b000000 0xc5------ 1000 0xc5
327804 W 0x00b000000 0xca------ 1000 0xca
328972 W 0x00b000000 0xdb------ 1000 0xdb
331080 W 0x00b000000 0xec------ 1000 0xec
333188 W 0x00b000000 0xfd------- 1000 0xec
FILTER ACCESS W RD RI
522 524 526

FIG. 9

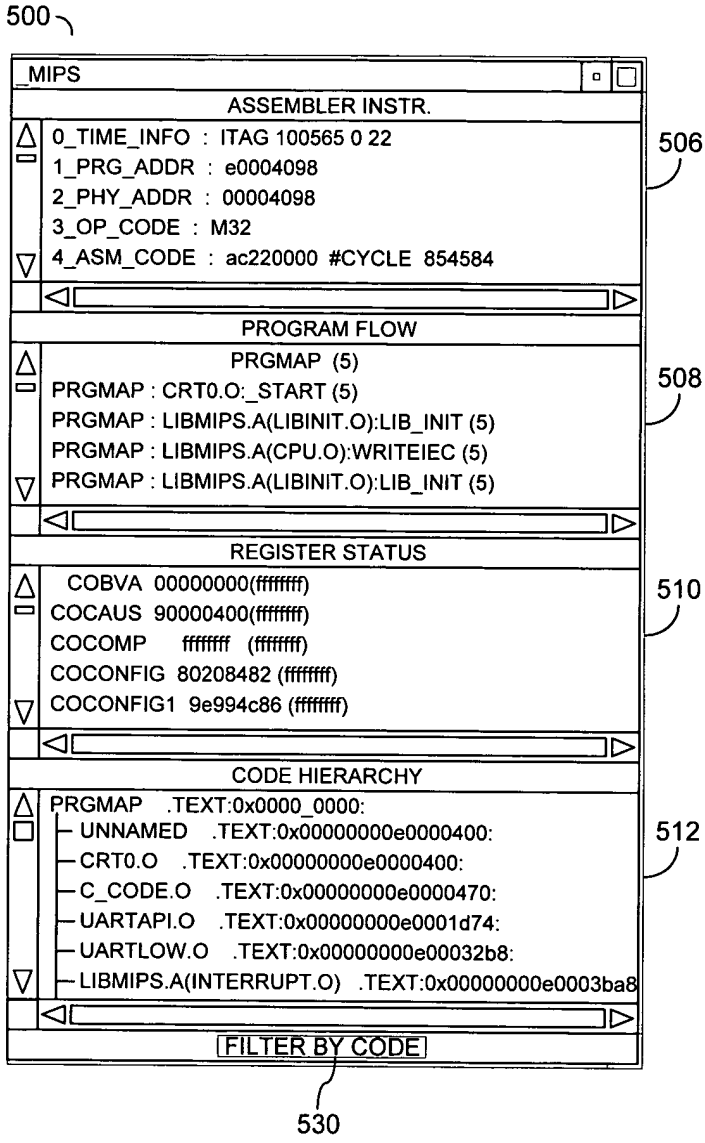
500
_MIPS
ASSEMBLER INSTR.
0_TIME_INFO : ITAG 100565 0 22
1_PRG_ADDR : e0004098
2_PHY_ADDR : 00004098
3_OP_CODE : M32
4_ASM_CODE : ac220000 #CYCLE 854584
506
PROGRAM FLOW
PRGMAP (5)
PRGMAP : CRT0.O:_START (5)
PRGMAP : LIBMIPS.A(LIBINIT.O):LIB_INIT (5)
PRGMAP : LIBMIPS.A(CPU.O):WRITEIEC (5)
PRGMAP : LIBMIPS.A(LIBINIT.O):LIB_INIT (5)
508
REGISTER STATUS
COBVA 00000000(ffffffff)
COCAUS 90000400(ffffffff)
COCOMP ffffffff (ffffffff)
COCONFIG 80208482 (ffffffff)
COCONFIG1 9e994c86 (ffffffff)
510
CODE HIERARCHY
PRGMAP .TEXT:0x0000_0000:
UNNAMED .TEXT:0x00000000e0000400:
CRT0.O .TEXT:0x00000000e0000400:
C_CODE.O .TEXT:0x00000000e0000470:
UARTAPI.O .TEXT:0x00000000e0001d74:
UARTLOW.O .TEXT:0x00000000e00032b8:
LIBMIPS.A(INTERRUPT.O) .TEXT:0x00000000e0003ba8
512
FILTER BY CODE
530

FIG. 10